



DDC S9700-23D Programming Guide

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DDC S9700-23D Programming Guide

Revision 1.0

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Feb. 03, 2020

UfiSpace Technology Corporation

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Revision History

Date	Rev	Author	Summary of Change
Feb 03, 2020	R1.0	Tom Chen	First Draft Release.

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1 Overview

This document describes the programming interfaces of the Distributed Disaggregated Chassis (DDC) Routing System, S9700-23D router, designed for telco service application.

The S9700-23D is the best of breed robust, flexible and carrier-grade Distributed Disaggregated Chassis (DDC) line card white box router that can be deployed in the core or edge to transport services over a scalable next-gen service provider network. Equipped with 400GE service and fabric ports, the S9700-23D enables fault and performance monitoring, non-stop routing support for control and data plane, and comprehensive high-availability networks.

The S9700-23D can be positioned as standalone or coupled with the S9705-48D fabric white box router in small, medium, and large clusters enabling 4Tb to 192Tb switching capacity. By connecting to the S9705-48D (fabric), it scales out not only economically and rapidly, but it also brings down the total cost of ownership.

The DDC Routing System adopts the innovated discrete Network Cloud Processor (NCP) and Network Cloud Fabric (NCF) building blocks providing flexibility to core router needs in the industry, integral to Ethernet switching performance and intelligence to networks while minimizing the network complexity.

1.1 Physical Overview

Front View



Rear View

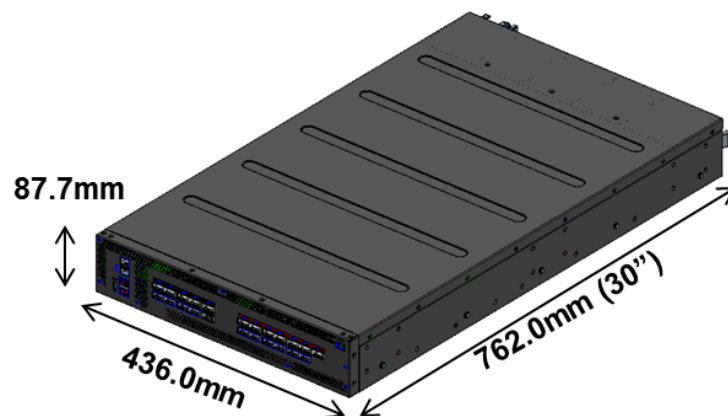


1.2 Feature Summary

- 1+1 Redundant power supply unit
 - 2000W output
 - 90~264VAC/-40~-72VDC input
 - Field replaceable
- 3+1 Redundant fan module
 - 16000 RPM
 - Front to Back air flow
 - Field replaceable
- Ethernet I/O ports:
 - 23 x 400GE QSFPDD ports
- Front/Rear panel LED indicators:
 - 2 x power status LED
 - 1 x FAN status LED
 - 1 x system status LED
 - Per port link status LED
 - Per port FAN status LED (Rear panel on each FRU)
 - Per port PSU status LED (Rear panel on each FRU)
- Management interfaces:
 - 1 x GE OOB management port (CPU)
 - 1 x USB2.0 Type-A general purpose port
 - 1 x RS232 console port in RJ45 form factor
 - 1 x USB console port in Micro USB form factor
 - 1 x tact switch for system reset/reload default configuration
 - 2 x 10G SFP+ management ports

1.3 Mechanical Outline

S9700-23D is designed to meet cabinet with 19" depth installation requirement. This 2RU system mechanical dimension is: 436mm(W) x 762mm(D) x 87.7mm(H)



1.4 Front & Real Panel Design

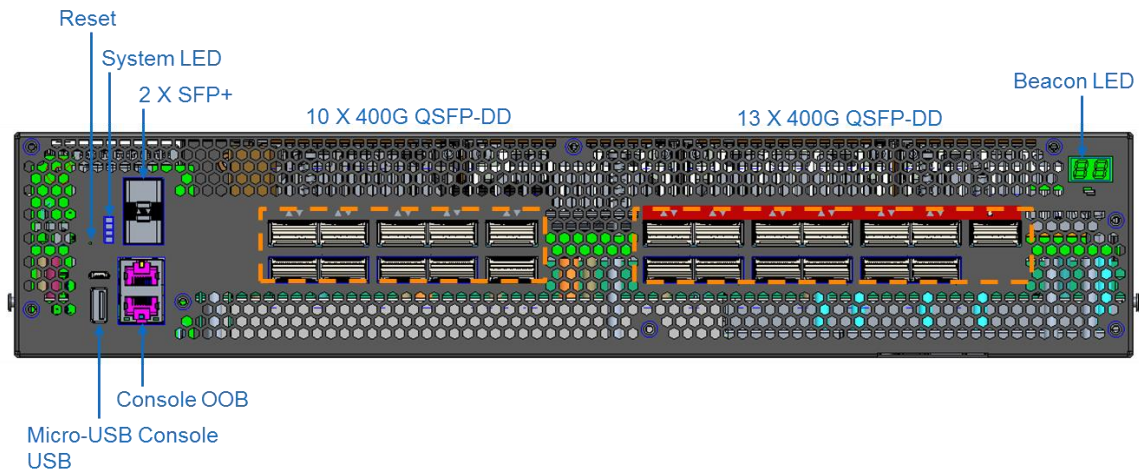
S9700-23D front panel IO ports & LED include below functionalities :

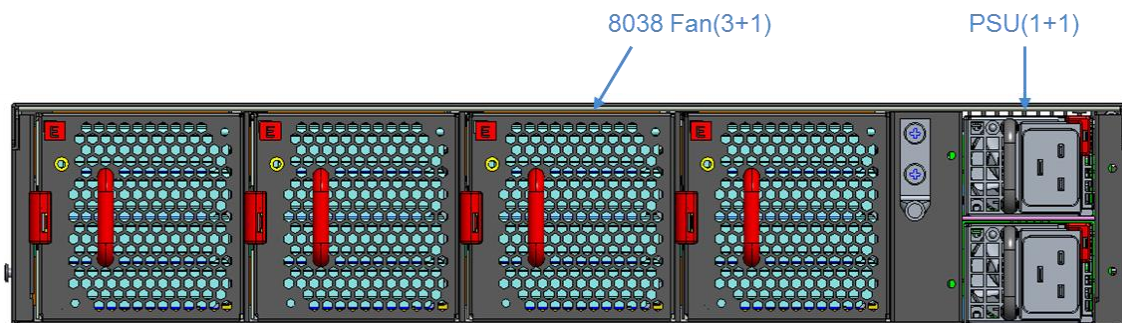
- System status LED
- ✓ Power status LED
- ✓ FAN status LED
- Ethernet ports LED
- ✓ OOB copper ports LED
- ✓ Data traffic fiber ports LED
- Management ports (Share between CPU and BMC)
- ✓ 1x OOB port
- ✓ 1x Type A USB port
- ✓ 1x console port in RJ45
- ✓ 1x console port in Micro-USB
- Ethernet data ports
- ✓ 23x 400GE QSFPDD ports

S9700-23D real panel design:

- FAN status LED
- PSU status LED

Detailed IO arrangement is shown as below :





1.5 LED Indicators

The system status and stacking LED are placed on main board.

LED Indication	Behavior	Description
SYS	OFF	No power
	Solid Green	Host CPU/BMC is up
	Solid Amber	Power is up but Host CPU/BMC is not up
FAN	OFF	Fans are not initialized
	Solid Green	All Fans are work normal
	Solid Amber	Fan fail : one or more Fans need service
PS1	OFF	No power
	Solid Green	PSU1 is work normal
	Solid Amber	PSU1 fail (PSU1 need service)
PS2	OFF	No power
	Solid Green	PSU2 is work normal
	Solid Amber	PSU2 fail (PSU2 need service)

The platform will have 2 green LEDs integrated in the front panel management RJ45 port.

LED Indication	Behavior	Description
OOB	OFF	No power
	Solid Green	1G link-up
	Blinking Green	1G TX/RX activity
	Solid Amber	10M/100M link-up

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	Blinking Amber	10M/100M TX/RX activity
--	----------------	-------------------------

The following table shows the 10G/400G LED definitions:

Location	LED Indication	Color	Behavior	Description
SFP+ ports	Link/Act/Speed of 10G	Green	Solid	Link up
			Blinking	Packet transmitting or receiving
			Off	No link or port disable
NIF QSFPDD	Link/Act/Speed	Green	Solid	Link up at 400G
			Blinking	Packet transmitting or receiving at 400G
			Off	No link or port disable
		Yellow	Solid	Link up at 200G
			Blinking	Packet transmitting or receiving at 200G
			Off	No link or port disable
FAB QSFPDD	Link/Act/Speed	Green	Solid	Link up at 400G
			Blinking	Packet transmitting or receiving at 400G
			Off	No link or port disable
		Red	Solid	Identify potential fail port
		Blue	Solid	Management to locate switch

1.6 Network Ports

1.6.1 Ports Assignment

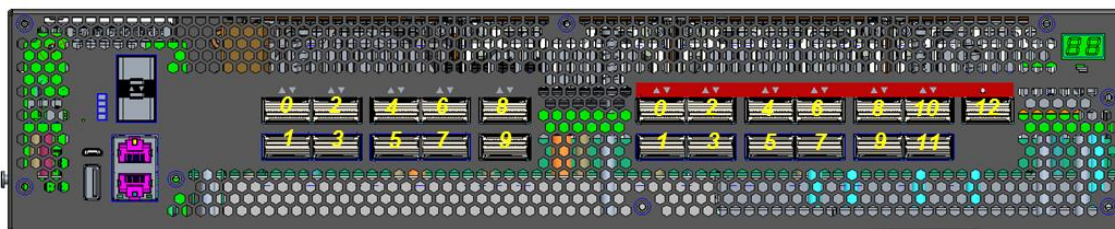


Table below shows the bit stream0 for NIF QSFPDD:

Front Panel Port Number	Bit Number	Function	Bit Value	Color	Bit Value	Color
P9	0	200G Link/ACT	1	Yellow	0	Off

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	1	400G Link/ACT	1	Green	0	Off
P8	2	200G Link/ACT	1	Yellow	0	Off
	3	400G Link/ACT	1	Green	0	Off
P7	4	200G Link/ACT	1	Yellow	0	Off
	5	400G Link/ACT	1	Green	0	Off
P6	6	200G Link/ACT	1	Yellow	0	Off
	7	400G Link/ACT	1	Green	0	Off
P5	8	200G Link/ACT	1	Yellow	0	Off
	9	400G Link/ACT	1	Green	0	Off
P4	10	200G Link/ACT	1	Yellow	0	Off
	11	400G Link/ACT	1	Green	0	Off
P3	12	200G Link/ACT	1	Yellow	0	Off
	13	400G Link/ACT	1	Green	0	Off
P2	14	200G Link/ACT	1	Yellow	0	Off
	15	400G Link/ACT	1	Green	0	Off
P1	16	200G Link/ACT	1	Yellow	0	Off
	17	400G Link/ACT	1	Green	0	Off
P0	18	200G Link/ACT	1	Yellow	0	Off
	19	400G Link/ACT	1	Green	0	Off



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1.6.2 Ports mapping

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Front Panel				MAC			
Connector		Physical port	Lane	Host side			
				TX_Lane (NIF/FAB)	TX polarity swap (Y/N)	RX_Lane (NIF/FAB)	RX polarity swap (Y/N)
Top Side	2x1 QSPDD#0	0	0	NIF_0	Y	NIF_0	Y
			1	NIF_1	Y	NIF_1	
			2	NIF_2	Y	NIF_2	
			3	NIF_3	Y	NIF_3	
			4	NIF_4	Y	NIF_4	Y
			5	NIF_5		NIF_5	
			6	NIF_6	Y	NIF_6	Y
			7	NIF_7		NIF_7	Y
		2	0	NIF_16	Y	NIF_16	
			1	NIF_17	Y	NIF_17	Y
			2	NIF_18	Y	NIF_18	
			3	NIF_19	Y	NIF_19	Y
			4	NIF_20	Y	NIF_20	Y
			5	NIF_21		NIF_21	
			6	NIF_22	Y	NIF_22	Y
			7	NIF_23		NIF_23	
Bottom Side	2x1 QSPDD#1	1	0	NIF_8	Y	NIF_8	
			1	NIF_9		NIF_9	
			2	NIF_10	Y	NIF_10	
			3	NIF_11		NIF_11	Y
			4	NIF_12		NIF_12	Y
			5	NIF_13	Y	NIF_13	
			6	NIF_14		NIF_14	Y
			7	NIF_15	Y	NIF_15	
		3	0	NIF_24		NIF_24	
			1	NIF_25	Y	NIF_25	
			2	NIF_26		NIF_26	
			3	NIF_27	Y	NIF_27	Y
			4	NIF_28	Y	NIF_28	Y
			5	NIF_29		NIF_29	
			6	NIF_30	Y	NIF_30	Y
			7	NIF_31		NIF_31	
Top Side	2x1 QSPDD#2	4	0	NIF_32	Y	NIF_32	
			1	NIF_33	Y	NIF_33	
			2	NIF_34		NIF_34	
			3	NIF_35	Y	NIF_35	
			0	NIF_36	Y	NIF_36	Y
			1	NIF_37		NIF_37	
			2	NIF_38	Y	NIF_38	Y
			3	NIF_39		NIF_39	
		6	0	NIF_88		NIF_88	Y
			1	NIF_89	Y	NIF_89	
			2	NIF_90	Y	NIF_90	
			3	NIF_91	Y	NIF_91	Y
			0	NIF_92	Y	NIF_92	Y
			1	NIF_93		NIF_93	Y
			2	NIF_94	Y	NIF_94	Y
			3	NIF_95		NIF_95	

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Bottom Side	2x1 QSFPDD#3	5	0	NIF 40		NIF 40	
			1	NIF 41		NIF 41	Y
			2	NIF 42		NIF 42	
			3	NIF 43	Y	NIF 43	Y
			0	NIF 44	Y	NIF 44	
			1	NIF 45		NIF 45	Y
			2	NIF 46	Y	NIF 46	
			3	NIF 47		NIF 47	
		7	0	NIF 80		NIF 80	
			1	NIF 81	Y	NIF 81	
			2	NIF 82		NIF 82	
			3	NIF 83	Y	NIF 83	
			0	NIF 84	Y	NIF 84	Y
			1	NIF 85		NIF 85	
			2	NIF 86	Y	NIF 86	Y
			3	NIF 87		NIF 87	
Top Side	2x1 QSFPDD#4	8	0	NIF 72	Y	NIF 72	
			1	NIF 73	Y	NIF 73	Y
			2	NIF 74	Y	NIF 74	
			3	NIF 75		NIF 75	
			0	NIF 76	Y	NIF 76	Y
			1	NIF 77		NIF 77	
			2	NIF 78	Y	NIF 78	Y
			3	NIF 79		NIF 79	
Bottom Side	2x1 QSFPDD#5	9	0	NIF 64	Y	NIF 64	
			1	NIF 65		NIF 65	
			2	NIF 66	Y	NIF 66	
			3	NIF 67		NIF 67	
			0	NIF 68	Y	NIF 68	
			1	NIF 69		NIF 69	Y
			2	NIF 70		NIF 70	
			3	NIF 71	Y	NIF 71	Y
Top Side	1x2 QSFPDD#0	0	0	FAB 57	Y	FAB 56	
			1	FAB 56		FAB 57	
			2	FAB 58		FAB 58	
			3	FAB 59	Y	FAB 59	
			4	FAB 61	Y	FAB 60	Y
			5	FAB 62		FAB 61	
			6	FAB 60	Y	FAB 62	Y
			7	FAB 63	Y	FAB 63	
		2	0	FAB 72	Y	FAB 72	
			1	FAB 75	Y	FAB 73	
			2	FAB 74	Y	FAB 74	Y
			3	FAB 73	Y	FAB 75	
			4	FAB 76	Y	FAB 76	Y
			5	FAB 79		FAB 77	
			6	FAB 78	Y	FAB 78	
			7	FAB 77		FAB 79	

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Bottom Side	1x2 QSPDD#1	1	0	FAB 66		FAB 64	
			1	FAB 67		FAB 65	Y
			2	FAB 65	Y	FAB 66	
			3	FAB 64		FAB 67	Y
			4	FAB_70	Y	FAB 68	Y
			5	FAB_71		FAB 69	
			6	FAB 69		FAB 70	Y
			7	FAB 68	Y	FAB 71	
		3	0	FAB 81	Y	FAB 80	
			1	FAB 83		FAB 81	
			2	FAB 82		FAB 82	
			3	FAB 80		FAB 83	
			4	FAB 84	Y	FAB 84	
			5	FAB 86	Y	FAB 85	Y
			6	FAB 85		FAB 86	
			7	FAB 87		FAB 87	Y
Top Side	1x2 QSPDD#2	4	0	FAB 90		FAB 88	Y
			1	FAB 88	Y	FAB 89	
			2	FAB 89	Y	FAB 90	
			3	FAB 91		FAB 91	
			4	FAB_95	Y	FAB 92	Y
			5	FAB_94		FAB 93	Y
			6	FAB 92		FAB 94	
			7	FAB 93	Y	FAB 95	Y
		6	0	FAB 107	Y	FAB 104	
			1	FAB 105		FAB 105	
			2	FAB 104		FAB 106	Y
			3	FAB_16	Y	FAB 107	Y
			4	FAB 108		FAB 108	
			5	FAB 111	Y	FAB 109	Y
			6	FAB 109	Y	FAB 110	Y
			7	FAB 110		FAB 111	Y
Bottom Side	1x2 QSPDD#3	5	0	FAB 98		FAB 96	Y
			1	FAB 99	Y	FAB 97	
			2	FAB 97		FAB 98	Y
			3	FAB 96	Y	FAB 99	Y
			4	FAB 103	Y	FAB 100	
			5	FAB_100		FAB_101	Y
			6	FAB_102		FAB_102	Y
			7	FAB 101	Y	FAB 103	Y
		7	0	FAB 50	Y	FAB 48	
			1	FAB 48	Y	FAB 49	Y
			2	FAB 49		FAB 50	Y
			3	FAB 51	Y	FAB 51	Y
			4	FAB 53	Y	FAB 52	Y
			5	FAB 54		FAB 53	Y
			6	FAB 55	Y	FAB 54	
			7	FAB 52		FAB 55	

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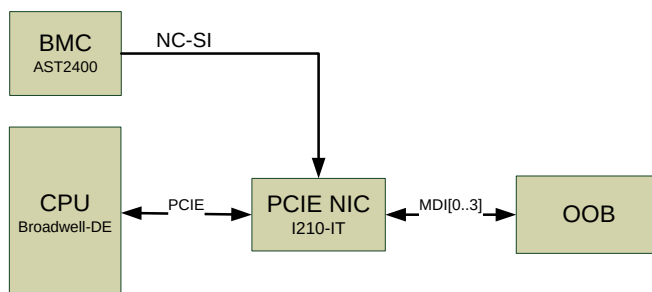
Top Side	1x2 QSFPDD#4	8	0	FAB_40		FAB_40	
			1	FAB_42	Y	FAB_41	
			2	FAB_43	Y	FAB_42	Y
			3	FAB_41		FAB_43	Y
			4	FAB_45	Y	FAB_44	Y
			5	FAB_46		FAB_45	Y
			6	FAB_44		FAB_46	Y
			7	FAB_47	Y	FAB_47	
		10	0	FAB_25	Y	FAB_24	Y
			1	FAB_24		FAB_25	Y
			2	FAB_26	Y	FAB_26	
			3	FAB_27	Y	FAB_27	
			4	FAB_31		FAB_28	
			5	FAB_29		FAB_29	
			6	FAB_30	Y	FAB_30	
			7	FAB_28	Y	FAB_31	
Bottom Side	1x2 QSFPDD#5	9	0	FAB_32	Y	FAB_32	Y
			1	FAB_34		FAB_33	
			2	FAB_35		FAB_34	Y
			3	FAB_33		FAB_35	
			4	FAB_36		FAB_36	
			5	FAB_39	Y	FAB_37	Y
			6	FAB_37	Y	FAB_38	Y
			7	FAB_38		FAB_39	Y
		11	0	FAB_19		FAB_16	Y
			1	FAB_16	Y	FAB_17	
			2	FAB_18	Y	FAB_18	Y
			3	FAB_17	Y	FAB_19	
			4	FAB_22		FAB_20	
			5	FAB_23	Y	FAB_21	Y
			6	FAB_20		FAB_22	Y
			7	FAB_21	Y	FAB_23	Y
Top Side	1x2 QSFPDD#6	12	0	FAB_10		FAB_8	
			1	FAB_9	Y	FAB_9	Y
			2	FAB_8		FAB_10	
			3	FAB_11	Y	FAB_11	Y
			4	FAB_14	Y	FAB_12	
			5	FAB_15	Y	FAB_13	
			6	FAB_13		FAB_14	
			7	FAB_12		FAB_15	

1.7 OOB Ports

The S9700-23D router includes 1 standard GE RJ45 port for out of band (OOB) management, share by CPU and BMC. It supports the IEEE 802.3 specification for 10/100/1000Mbps operation.

PCIe interface is routed between CPU & NIC I210-IT, OOB supports 10/100/1000Mbps operation. NC-SI is connected between BMC & NIC I210-IT, OOB speed is limited to 100Mbps in this case.

OOB to BMC can be disabled by BIOS.



1.8 Console Port

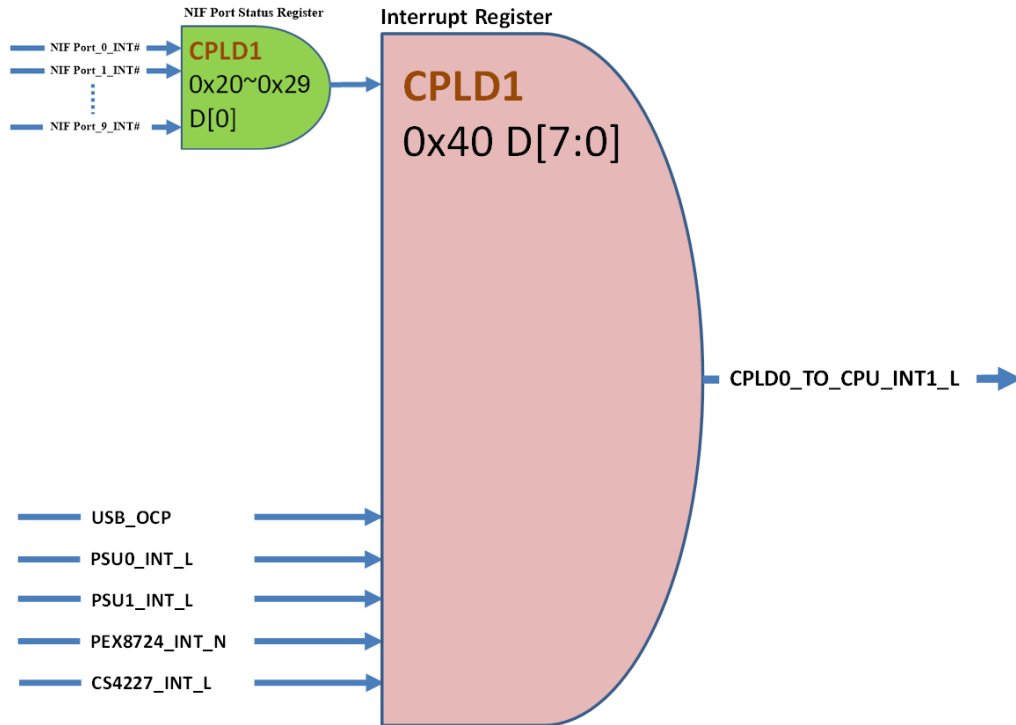
Two console ports available for S9700-23D systems access, both of them can be used for CPU or BMC access. The pin definition of the RS232 console port is shown as below. Pin3 is the TX signal from internal processor to external RS232 interface, and Pin6 is the RX signal from external RS232 interface to internal processor. The default baud rate is 115200 bps.

PIN #	Definition	Direction	Note
1	NC		
2	NC		
3	UART_TXD	Out	Console TX
4	GND		
5	GND		
6	UART_RXD	In	Console RX
7	GND		
8	GND		

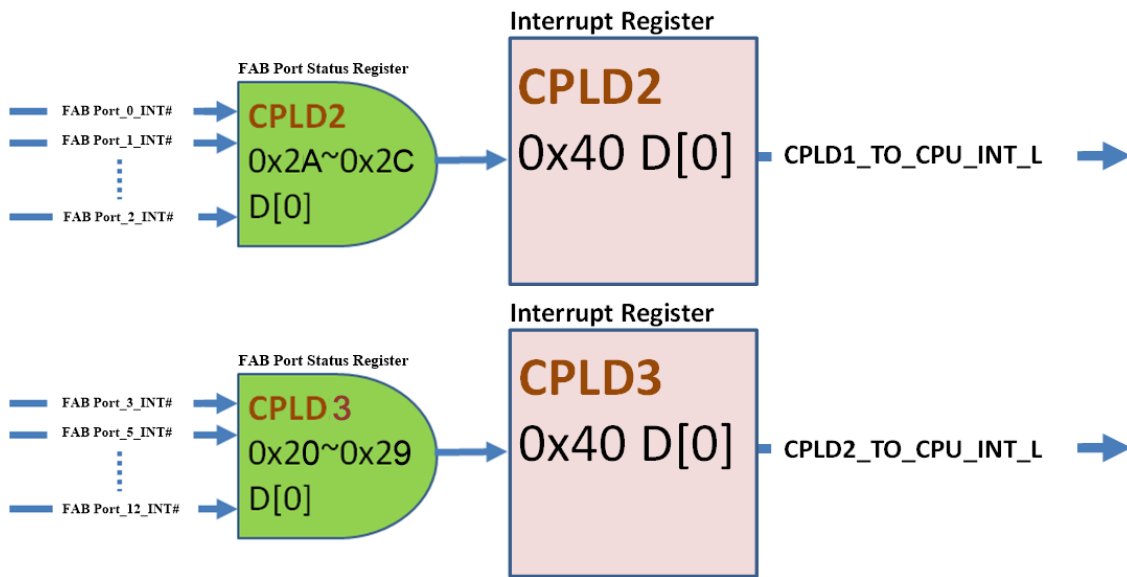
1.9 Interrupt Tree

1.9.1 CPLD1 Interrupt

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1.9.2 CPLD2/3 Interrupt



2 Main System

This section describes in software view to access the system key interfaces in main system.

2.1 Memory and I/O Mapping

Fixed I/O ranges decoded by Broadwell-DE:

I/O Address	Read Target	Write Target	Internal Unit
00h-08h	DMA controller	DMA controller	DMA
09h-0Eh	reserved	DMA controller	DMA
0Fh	DMA controller	DMA controller	DMA
10h-18h	DMA controller	DMA controller	DMA
19h-1Eh	reserved	DMA controller	DMA
1Fh	DMA controller	DMA controller	DMA
20h-21h	Interrupt controller	Interrupt controller	interrupt
24h-25h	Interrupt controller	Interrupt controller	interrupt
28h-29h	Interrupt controller	Interrupt controller	interrupt
2Ch-2Dh	Interrupt controller	Interrupt controller	interrupt
2Eh-2Fh	LPC SIO	LPC SIO	Forwarded to LPC
30h-31h	Interrupt controller	Interrupt controller	interrupt
34h-35h	Interrupt controller	Interrupt controller	interrupt
38h-39h	Interrupt controller	Interrupt controller	interrupt
3Ch-3Dh	Interrupt controller	Interrupt controller	interrupt
40h-42h	Timer/Counter	Timer/Counter	PIT
43h	reserved	Timer/Counter	PIT
4Eh-4Fh	LPC SIO	LPC SIO	Forwarded to LPC
50h-52h	Timer/Counter	Timer/Counter	PIT
53h	reserved	Timer/Counter	PIT
60h	microcontroller	microcontroller	Forwarded to LPC
61h	NMI controller	NMI controller	Processor I/F
62h	microcontroller	microcontroller	Forwarded to LPC
64h	microcontroller	microcontroller	Forwarded to LPC
66h	microcontroller	microcontroller	Forwarded to LPC
70h	reserved	NMI and RTC controller	RTC
71h	RTC controller	RTC controller	RTC
72h	RTC controller	NMI and RTC controller	RTC
73h	RTC controller	RTC controller	RTC
74h	RTC controller	NMI and RTC controller	RTC
75h	RTC controller	RTC controller	RTC
76h	RTC controller	NMI and RTC controller	RTC
77h	RTC controller	RTC controller	RTC

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80h	DMA controller, LPC, PCI or PCIe	DMA controller, LPC, PCI or PCIe	DMA
81h-83h	DMA controller	DMA controller	DMA
84h-86h	DMA controller	DMA controller, LPC, PCI or PCIe	DMA
87h	DMA controller	DMA controller	DMA
88h	DMA controller	DMA controller, LPC, PCI or PCIe	DMA
89h-8Bh	DMA controller	DMA controller	DMA
8Ch-8Eh	DMA controller	DMA controller, LPC, PCI or PCIe	DMA
8Fh	DMA controller	DMA controller	DMA
90h-91h	DMA controller	DMA controller	DMA
92h	Reset generator	Reset generator	Processor I/F
93h-9Fh	DMA controller	DMA controller	DMA
A0h-A1h	Interrupt controller	Interrupt controller	interrupt
A4h-A5h	Interrupt controller	Interrupt controller	interrupt
A8h-A9h	Interrupt controller	Interrupt controller	interrupt
ACh-ADh	Interrupt controller	Interrupt controller	interrupt
B0h-B1h	Interrupt controller	Interrupt controller	interrupt
B2h-B3h	Power management	Power management	Power management
B4h-B5h	Interrupt controller	Interrupt controller	interrupt
B8h-B9h	Interrupt controller	Interrupt controller	interrupt
BCh-BDh	Interrupt controller	Interrupt controller	interrupt
C0h-D1h	DMA controller	DMA controller	DMA
D2h-DDh	reserved	DMA controller	DMA

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DEh-DFh	DMA controller	DMA controller	DMA
F0h	Ferr#/interrupt controller	Ferr#/interrupt controller	Processor I/F
170h-177h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
1F0h-1F7h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
200h-207h	Gameport low	Gameport low	Forwarded to LPC
208h-20Fh	Gameport high	Gameport high	Forwarded to LPC
376h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
3F6h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
4D0h-4D1h	Interrupt controller	Interrupt controller	interrupt
CF9h	Reset generator	Reset generator	Processor I/F

Fixed I/O ranges decoded by Broadwell-DE:

Range name	Mappable	Size (bytes)	Target
ACPI	Anywhere in 64KB I/O space	6	Power management
IDE bus master	Anywhere in 64KB I/O space	1. 16 or 32 2. 16	1. SATA host controller #1, #2 2. IDE-R
Native IDE command	Anywhere in 64KB I/O space	8	1. SATA host controller #1, #2 2. IDE-R
Native IDE control	Anywhere in 64KB I/O space	4	1. SATA host controller #1, #2 2. IDE-R
SATA index/data pair	Anywhere in 64KB I/O space	1 6	1. SATA host controller #1, #2 2. IDE-R
SMBus	Anywhere in 64KB I/O space	3	SMB unit
TCO	96 bytes above ACPI base	3	TCO unit
GPIO	Anywhere in 64KB I/O space	128	GPIO unit
Parallel port	3 ranges in 64KB I/O space	8	LPC peripheral
Serial port 1	8 ranges in 64KB I/O space	8	LPC peripheral
Serial port 2	8 ranges in 64KB I/O space	8	LPC peripheral
Floppy disk controller	2 ranges in 64KB I/O space	8	LPC peripheral
LAN	Anywhere in 64KB I/O space	3	LAN unit

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LPC generic 1	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
LPC generic 2	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
LPC generic 3	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
LPC generic 4	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
I/O trapping ranges	Anywhere in 64KB I/O space	1 to 256	Trap on backbone
PCI bridge	Anywhere in 64KB I/O space	I/O base/limit	PCI bridge
PCI-E root ports	Anywhere in 64KB I/O space	I/O base/limit	PCI-E root ports 1-8
KT	Anywhere in 64KB I/O space	8	KT

Memory decode ranges from processor perspective:

Memory range	target	Dependency/comments
0000 0000h-000D FFFFh 0010 0000h-TOM	Main memory	TOM registers in host controller
000E 0000h-000E FFFFh	LPC or SPI	Bit 6 in BIOS decode enable register is set
000F 0000h-000F FFFFh	LPC or SPI	Bit 7 in BIOS decode enable register is set
FEC_ 000h-FEC_ 040h	IOx APCI inside broadwell-de SoC	__ is controlled using APIC range select (ASEL) field and APIC enable (AEN) bit.
FEC1 0000h-FEC1 7FFFh	PCI-E port 1	PCI-E root port 1 I/OxAPIC enable (PAE) set
FEC1 8000h-FEC1 FFFFh	PCI-E port 2	PCI-E root port 2 I/OxAPIC enable (PAE) set
FEC2 0000h-FEC2 7FFFh	PCI-E port 3	PCI-E root port 3 I/OxAPIC enable (PAE) set
FEC2 8000h-FEC2 FFFFh	PCI-E port 4	PCI-E root port 4 I/OxAPIC enable (PAE) set
FEC3 0000h-FEC3 7FFFh	PCI-E port 5	PCI-E root port 5 I/OxAPIC enable (PAE) set
FEC3 8000h-FEC3 FFFFh	PCI-E port 6	PCI-E root port 6 I/OxAPIC enable (PAE) set
FEC4 0000h-FEC4 7FFFh	PCI-E port 7	PCI-E root port 7 I/OxAPIC enable (PAE) set
FEC4 8000h-FEC4 FFFFh	PCI-E port 8	PCI-E root port 8 I/OxAPIC enable (PAE) set
FFC0 0000h-FFC7 FFFFh	LPC or SPI (or PCI)	Bit 8 in BIOS decode enable register is set
FFC8 0000h-FFCF FFFFh	LPC or SPI (or PCI)	Bit 9 in BIOS decode enable register is set
FFD0 0000h-FFD7 FFFFh	LPC or SPI (or PCI)	Bit 10 in BIOS decode enable register is set
FFD8 0000h-FFDF FFFFh	LPC or SPI (or PCI)	Bit 11 in BIOS decode enable register is set
FFE0 0000h-FFE7 FFFFh	LPC or SPI (or PCI)	Bit 12 in BIOS decode enable register is set
FFE8 0000h-FFE7 FFFFh	LPC or SPI (or PCI)	Bit 13 in BIOS decode enable register is set
FFF0 0000h-FFF7 FFFFh	LPC or SPI (or PCI)	Bit 14 in BIOS decode enable register is set
FFF8 0000h-FFFF FFFFh	LPC or SPI (or PCI)	Always enabled.
FF70 0000h-FF7F FFFFh	LPC or SPI (or PCI)	Bit 3 in BIOS Decode Enable register is set
FF60 0000h-FF6F FFFFh	LPC or SPI (or PCI)	Bit 2 in BIOS Decode Enable register is set
FF50 0000h-FF5F FFFFh	LPC or SPI (or PCI)	Bit 1 in BIOS Decode Enable register is set
FF40 0000h-FF4F FFFFh	LPC or SPI (or PCI)	Bit 0 in BIOS Decode Enable register is set
128 KB anywhere in 4 GB	Integrated LAN Controller	Enable using BAR in D25:F0
4 KB anywhere in 4 GB	Integrated LAN Controller	Enable using BAR in D25:F0
1 KB anywhere in 4 GB	USB EHCI Controller #1	Enable using standard PCI mechanism
64 KB anywhere in 4 GB	USB xHCI Controller	Enable using standard PCI mechanism

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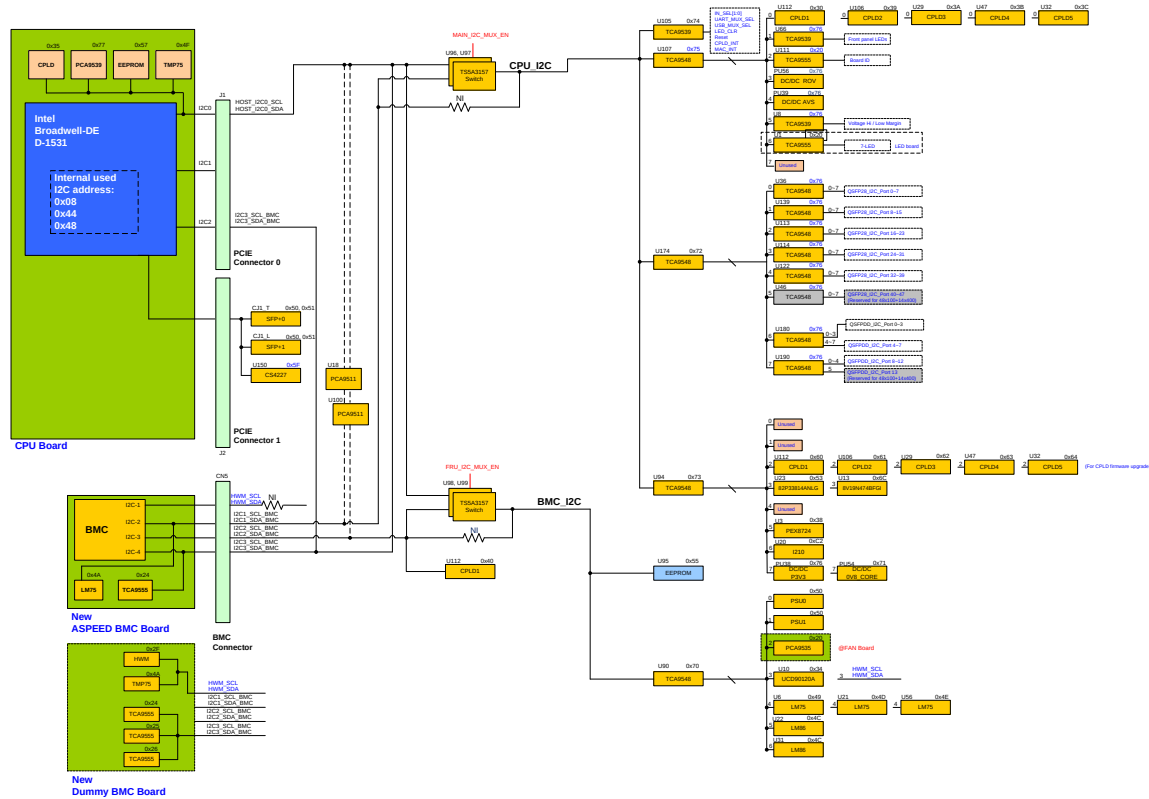
FED0 X000h–FED0 X3FFh	High Precision Event	BIOS determines “fixed” location which is
FED4 0000h–FED4 FFFFh	TPM on LPC	None
Memory Base/Limit	PCI Bridge	Enable using standard PCI mechanism
Prefetchable Memory	PCI Bridge	Enable using standard PCI mechanism
64 KB anywhere in 4 GB range	LPC	LPC Generic Memory Range. Enable using setting bit[0] of the LPC Generic
32 Bytes anywhere in 64-bit	SMBus	Enable using standard PCI mechanism
2 KB anywhere above 64 KB	SATA Host Controller #1	AHCI memory-mapped registers. Enable
Memory Base/Limit	PCI Express* Root Ports 1-	Enable using standard PCI mechanism
Prefetchable Memory	PCI Express Root Ports 1-8	Enable using standard PCI mechanism
4 KB anywhere in 64-bit	Thermal Reporting	Enable using standard PCI mechanism
4 KB anywhere in 64-bit	Thermal Reporting	Enable using standard PCI mechanism
16 Bytes anywhere in 64-bit	Intel® MEI #1, #2	Enable using standard PCI mechanism
4 KB anywhere in 4 GB	KT	Enable using standard PCI mechanism
16 KB anywhere in 4 GB	Root Complex Register	Enable using setting bit[0] of the Root

2.1.1 SMBus

There is one SMBus, which is I2C compatible, on S9500-30XS controlled by CPU card. It is configured to operate in standard mode, 100KHz clock frequency. Four I2C buses from BMC are connected to switch board I2C devices with dedicated I2C mux.

I2C block diagram is shown as below:

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CPU_I2C Map:

I2C Bus	Name	Address		Device	Bit #	Function
CPU_I2C	I/O EXP	111-0100	0x74	TCA9539	0.7	8V19N474_INT
					0.6	UART_MUX1_SEL
					0.5	UART_MUX2_SEL
					0.4	USB_MUX_SEL
					0.3	HOST_TO_BMC_I2C_GPIO
					0.2	LED_CLR
					0.1	EXP_J2_PCIE_RST_L
					0.0	9539_J2_RST_L
					1.7	I210_RST_L
					1.6	I210_PE_RST_L
					1.5	OP2_INT_L
					1.4	CPLD01_TO_CPU_INT_L

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I2C Bus	Name	Address		Device	Bit #	Function
					1.3	CPLD2_TO_CPU_INT_L
					1.2	CPLD3_TO_CPU_INT_L
					1.1	CPLD4_TO_CPU_INT_L
					1.0	J2_INT_L
	I2C MUX	111-0001	0x75	TCA9548	--	CPLDs, System LEDs, Board ID, CPLDs DC/DC ROV, DC/DC AVS, Voltage Margin
	I2C MUX	111-0010	0x72	TCA9548	--	I2C of QSFP28 Port 1~40 I2C of QSFPDD Port 1~13
	I2C MUX	111-0011	0x73	TCA9548	--	CPLD upgrade Clock Gens. PCIE switch, PEX8716 Ethernet controller, I210 DC/DC P3V3, DC/DC 0V8_CORE
	Device				Ch #	Function
	TCA9548 0x75				Ch0	CPLD1~CPLD5 , 0x40, 0x39 ~ 0x3C
					Ch1	TCA9539, 0x76 Ch1.7: Unused Ch1.6: Unused Ch1.5: Unused Ch1.4: Unused Ch1.3: Unused Ch1.2: Unused Ch1.1: PSU0_PWROK Ch1.0: PSU1_PWROK Ch0.7: Unused Ch0.6: Unused Ch0.5: Unused Ch0.4: PSU0_LED_Y Ch0.3: PSU1_LED_Y Ch0.2: FAN_LED_Y Ch0.1: FAN_LED_EN Ch0.0: PSU0_LED_Y
					Ch2	TCA9555, 0x20 Ch1.7: Board_ID_3 Ch1.6: Board_ID_2 Ch1.5: Board_ID_1 Ch1.4: Board_ID_0 Ch1.3: HW_REV_1 Ch1.2: HW_REV_0 Ch1.1: Build_REV_1 Ch1.0: Build_REV_0 Ch0.7: Unused

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I2C Bus	Name	Address	Device	Bit #	Function
					Ch0.6: Unused Ch0.5: Unused Ch0.4: Unused Ch0.3: Unused Ch0.2: Unused Ch0.1: Unused Ch0.0: Unused
				Ch3	DC/DC ROV, 0x76
				Ch4	DC/DC AVS, 0x76
				Ch5	TCA9539, 0x76 Voltage High/Low margin test
				Ch6	TCA9548, 0x20 Beacon LED
				Ch7	Unused
	Device			Ch #	Function
				Ch0	TCA9548, 0x76 Ch0: NIF_QSFPDD Port 0 I2C Ch1: NIF_QSFPDD Port 1 I2C Ch2: NIF_QSFPDD Port 2 I2C Ch3: NIF_QSFPDD Port 3 I2C Ch4: NIF_QSFPDD Port 4 I2C Ch5: NIF_QSFPDD Port 5 I2C Ch6: NIF_QSFPDD Port 6 I2C Ch7: NIF_QSFPDD Port 7 I2C
				Ch1	TCA9548, 0x76 Ch0: NIF_QSFPDD Port 8 I2C Ch1: NIF_QSFPDD Port 9 I2C Ch2: Reserved for NIF_QSFPDD 10 Ch3: Reserved for NIF_QSFPDD 11 Ch4: Unused Ch5: Unused Ch6: Unused Ch7: Unused
				Ch2	Unused
				Ch3	Unused
				Ch4	Unused
				Ch5	Unused
				Ch6	TCA9548, 0x76 Ch0: FAB_QSFPDD Port 0 I2C Ch1: FAB_QSFPDD Port 1 I2C

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I2C Bus	Name	Address		Device	Bit #	Function
						Ch2: FAB_QSFPDD Port 2 I2C Ch3: FAB_QSFPDD Port 3 I2C Ch4: FAB_QSFPDD Port 4 I2C Ch5: FAB_QSFPDD Port 5 I2C Ch6: FAB_QSFPDD Port 6 I2C Ch7: FAB_QSFPDD Port 7 I2C
					Ch7	TCA9548, 0x76 Ch0: FAB_QSFPDD Port 8 I2C Ch1: FAB_QSFPDD Port 9 I2C Ch2: FAB_QSFPDD Port 10 I2C Ch3: FAB_QSFPDD Port 11 I2C Ch4: FAB_QSFPDD Port 12 I2C Ch5: Reserved for FAB_QSFPDD 13 Ch6: Unused Ch7: Unused
	Device				Ch #	Function
	TCA9548 0x73				Ch0	Unused
					Ch1	Unused
					Ch2	CPLD1~CPLD5, 0x60~0x64 For CPLD firmware upgrade
					Ch3	Clock generators 82P33814ANLG, 0x53 8V19N474BFGI, 0x6C
					Ch4	Unused
					Ch5	PCIE Switch PEX8724, 0x38
					Ch6	Ethernet Controller I210, 0xC2
					Ch7	DC/DC P3V3, 0x76 DC/DC 0V8_CORE, 0x71

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BMC_I2C Map:

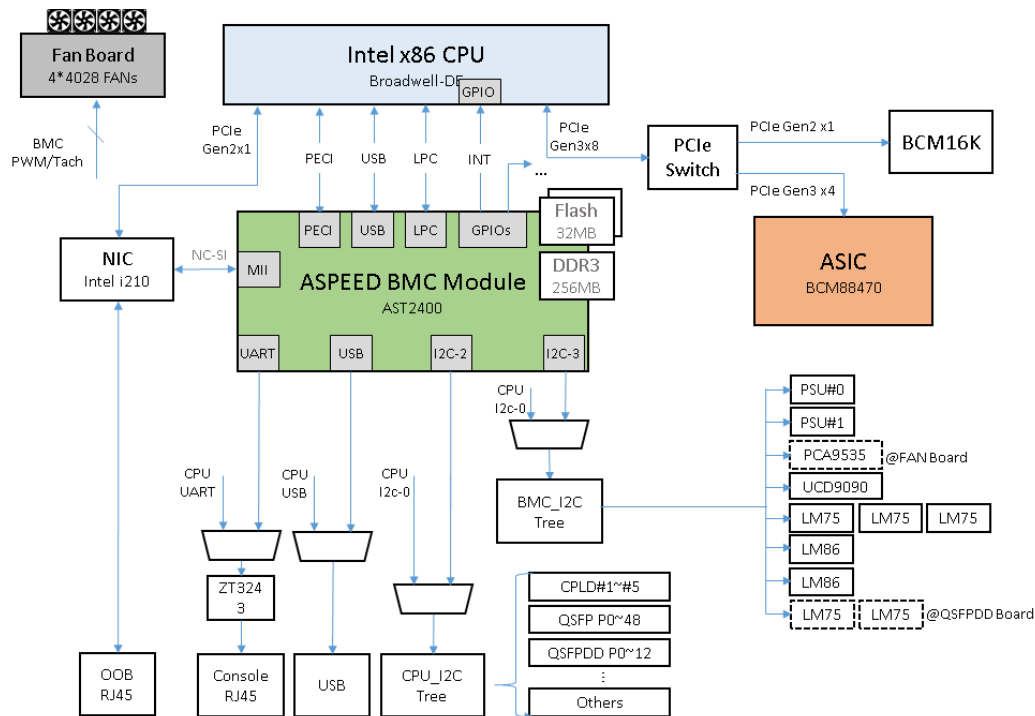
I2C Bus	Name	Address		Device	Bit #	Function
BMC_I2C	EEPROM	101-0101	0x55	M24128	--	Main Board EEPROM
	CPLD1	000-0100	0x40	CPLD	--	CPLD1
	I2C MUX	111-0000	0x70	TCA9548	--	FRU units, thermal sensors
	Device				Ch #	Function
	TCA9548 0x74				Ch0	PSU0, 0x50
					Ch1	PSU1, 0x50
					Ch2	PCA9535, 0x20 (at Fan board) Ch1.7: FAN4_DIR Ch1.6: FAN4_ABS Ch1.5: FAN4_LED_Y Ch1.4: FAN4_LED_G Ch1.3: FAN3_DIR Ch1.2: FAN3_ABS Ch1.1: FAN3_LED_Y Ch1.0: FAN3_LED_G Ch0.7: FAN2_DIR Ch0.6: FAN2_ABS Ch0.5: FAN2_LED_Y Ch0.4: FAN2_LED_G Ch0.3: FAN1_ABS Ch0.2: FAN1_ABS Ch0.1: FAN1_LED_Y Ch0.0: FAN1_LED_G
					Ch3	Voltage monitor UCD90120A, 0x34 HWM W83795, 0x2F
					Ch4	Thermal sensor LM75, 0x49 Thermal sensor LM75, 0x4D Thermal sensor LM75, 0x4E
					Ch5	Thermal sensor LM86, 0x4C
					Ch6	Thermal sensor LM86, 0x4C
					Ch7	reserved

CS4227_I2C Map:

I2C Bus	Name	Address		Device	Bit #	Function
CS4227_I2C	SFP+0	101-0000	0x50	SFP+	--	SFP+ Port 0
		101-0001	0x51			
	SFP+1	101-0000	0x50	SFP+	--	SFP+ Port 1
		101-0001	0x51			

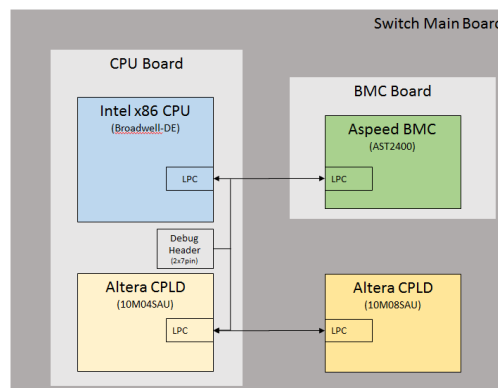
3 BMC sub-system

In S9700-23D project, base board management controller (BMC) autonomously monitors system's health including temperature, voltage, fan speed, etc. We use the DDR4 SO-DIMM connector as the BMC module connector. The BMC module connector is on the main board PCBA.:



3.1 LPC

Low-Pin-Count interface is an important interface for communication among Broadwell-DE, CPLD on CPU Board and BMC. The OS running in x86 use this interface to communicate with BMC's IPMI message handler. The connection topology is shown as below.



3.2 GPIO

AST2400 Integrates one set of Parallel GPIO Controller with maximum 216 control pins, which are 28 sets, to provide general-purpose input/output functions. All functional parallel GPIOs of S9700-23D router in different group are listed as below.

Group	Ball Name	Net Name	Direction	Function
GPIOB	GPIOB0	THERMAL_ALERT	input	Interrupt to BMC for thermal event
	GPIOB4	CPU_TH_RST_L	output	Reset of BCM88690
GPIOE	GPIOE2	PSU1_PWRON_L	input	PSU#0 Power On signal
	GPIOE3	BMC_TO_UCD_RST_L	output	Reset from BMC to UCD
GPIOF	GPIOF3	CPU_PRSENT_L	input	CPU card present signal
	GPIOF5	USB_MUX_SEL	output	USB Switch for CPU or BMC
GPIOK	GPIOK0	UART_MUX_SEL	output	Uart switch for CPU or BMC
	GPIOK1	P3V3_FAN_EN	output	Fan enable
	GPIOK2	FAN_STATUS_INT_L	input	Fan status interrupt
	GPIOK3	FP_BTN_UARTSEL_EN_L	output	Front panel uart switch
	GPIOK4	RST_CPU_PWRBTN_N	output	Reset from BMC to CPU
	GPIOK5	ALL_PWR_GOOD	input	All power good on BMC module card
	GPIOK6	PSU0_PRSENT_N	input	PSU#0 present signal
	GPIOK7	PSU0_PWROK	input	PSU#0 Power OK signal
GPIOI	GPIOI2	SYSTEM_LED_RST_L	input	System LED reset control
	GPIOI3	HOST_TO_BMC_I2C_GPIO	input	Reserved GPIO between CPU and BMC
	GPIOI4	MAIN_I2C_MUX_RST_L	input	I2C Switch for CPU or BMC
GPIOM	GPIOM0	HOST_TO_BMC_INT_L	input	Interrupt from CPU to BMC
	GPIOM1	BMC_TO_HOST_NMI	output	Interrupt from BMC to CPU
	GPIOM2	RST_BMC_TO_CPU_N	output	Reset from BMC to CPU

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	GPIOM4	P3V3_I2C_EN	output	I2C tree power enable
	GPIOM6	UCD9090_INT_L	input	Interrupt from UCD to BMC
	GPIOM7	UCD9090_CNTRL	output	UCD enable signal
GPIO P	GPIOP2	PSU0_PWRON_L	input	PSU#0 power OK signal
	GPIOP3	PSU0_INT_L	input	PSU#0 interrupt
	GPIOP4	PSU1_PWRON_L	input	PSU#1 power On signal
	GPIOP5	PSU1_PWROK	input	PSU#1 power OK signal
	GPIOP6	BMC_INT	output	Interrupt from BMC to CPU
	GPIOP7	PSU1_INT_L	input	PSU#1 interrupt

3.3 Base Board Management

BMC starts to configure, manage and monitor components through I2C, LPC, NC-SI interfaces. The following table lists these components and actions.

Interface	Component	IPMI device name	Configure
[0x74] I2C MUX TCA9548 #0	[0x50] PSU0_MCU	PSU0_FAN	Get speed
		PSU0_Temp	Get temperature/Set threshold value
	[0x50] PSU1_MCU	PSU1_FAN	Get speed
		PSU1_Temp	Get temperature/Set threshold value
	[0x20] PCA9535@FAN Board (FAN direction)	-	Get FAN direction
	[0x34] UCD90120	PERI_P3V3_VIN	Get voltage/Set threshold value
		P5V_SB_VIN	Get voltage/Set threshold value
		P3V8_BMC_VIN	Get voltage/Set threshold value
		P2V5_VIN	Get voltage/Set threshold value
		P3V3_BMC_VIN	Get voltage/Set threshold value
		ROV_CORE_VIN	Get voltage/Set threshold value
		P1V8_VIN	Get voltage/Set threshold value
		P1V2_VIN	Get voltage/Set threshold value
		P0V9_VIN	Get voltage/Set threshold value
		P0V88_VIN	Get voltage/Set threshold value

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		AVS_CORE_MON	Get voltage/Set threshold value
		OV8_CORE_MON	Get voltage/Set threshold value
	[0x49] LM75@ Main Board	Temp_BOARD1	Get temperature/Set threshold value
	[0x4D] LM75@ Main Board	Temp_BOARD2	Get temperature/Set threshold value
	[0x4E] LM75@ Main Board	Temp_BOARD3	Get temperature/Set threshold value
	[0x4C] LM86@ Main Board	Temp_MAC1	Get temperature/Set threshold value
	[0x4C] LM86@ Main Board	Temp_MAC2	Get temperature/Set threshold value
	[0x4D] LM75@QSFPDD	Temp_QSFP1	Get temperature/Set threshold value
	[0x4E] LM75@QSFPDD	Temp_QSFP2	Get temperature/Set threshold value
TACHO	TACHO#1 @bmc card	Fan0	Get speed
	TACHO#3 @bmc card	Fan1	Get speed
	TACHO#5 @bmc card	Fan2	Get speed
	TACHO#7 @bmc card	Fan3	Get speed
PECI	PECI	TEMP_CPU_PECI	Get temperature/Set threshold value
ADC	BMC integrated ADC #0	P3V15_LICELL	Get voltage/Set threshold value
	BMC integrated ADC #1	ADC_CPU_TEMP_SENSOR	Get temperature/Set threshold value
	BMC integrated ADC #2	HWM_VDD_CORE_VSENSE	Get voltage/Set threshold value
	BMC integrated ADC #4	HWM_P1V8_VSENSE	Get voltage/Set threshold value
	BMC integrated ADC #5	P3V3_VSENSE	Get voltage/Set threshold value
	BMC integrated ADC #6	HWM_P0V8_VSENSE	Get voltage/Set threshold value
	BMC integrated ADC #12	BMC_P1V26_VSENSE	Get voltage/Set threshold value
	BMC integrated ADC #13	BMC_P1V538_VSENSE	Get voltage/Set threshold value
	BMC integrated ADC #14	BMC_P3V3_VSENSE	Get voltage/Set threshold value
	BMC integrated ADC #15	BMC_P5V_VSENSE	Get voltage/Set threshold value

4 CPLD

4.1 CPU board CPLD Register Mapping and Description

Offset	Register	Description
0x00	Revision	Revision register
0x01	Status-0	Status register for reading input signals from BMC
0x02	Status-1	Status register for reading information of BIOS flash selection
0x03	Cntrl-0	Control register used to send signals to BMC
0x04	Cntrl-1	Control register used to send signals to BMC
0x05	Mask-0	
0x06	SKU ID	SKU ID register

CPU CPLD resistor description is shown as below:

Revision				
Offset = 0x00				
Bit	R/W	Name	Reset Value	Description
7:4	RO	Revision	0000	CPLD Revision Number, hardwired
3:0	RO	Revision	1011	CPLD Revision Number, hardwired

Status-0				
Offset = 0x01				
Bit	R/W	Name	Reset Value	Description
7	R/W	BMC_to_HOST_NMI_L	1	Non-maskable Interrupt Request to BMC
6	R/W	BMC_to_HOST_INT_L	1	Interrupt Request to BMC
5:0		Reserved	X	

Status-1				
Offset = 0x02				
Bit	R/W	Name	Reset Value	Description
7	RO	BIOS_MUXSEL	x	Actual value of BIOS_MUXSEL. If the Watchdog logic triggered, it will be different than CTRL-1[7]. Otherwise, it will be same value.
6:0		Reserved	X	

Cntrl-0				
Offset = 0x03				
Bit	R/W	Name	Reset Value	Description
7	R/W	HOST_to_MB_RST_L	1	Reset signal to reset the motherboard from CPU
6	R/W	HOST_to_MB_I2C_RST_L	1	
5	R/W	HOST_to_BMC_RST_L	1	
4	R/W	HOST_to_MM_INT_L	1	
3:0		Reserved	x	

Cntrl-1				
Offset = 0x04				
Bit	R/W	Name	Reset Value	Description
7	R/W	BIOS_MUX_SEL	0	This bit is not reset with a hardware reset. It will default to its value when power up, only. This value is used to write to the BIOS MUX selector when watchdog recovery is disabled (WDT_RCVRY_EN=0).
6:1		Reserved	x	
1	R/W	WDT_DOG_EN	1	This bit enables the Watchdog timer during boot process. The CPU must disable this bit right after it boots. It is enabled upon power up or sys_reset.
0	R/W	WDT_RCVRY_EN	1	This bit enables the watchdog recovery logic. It controls bios_mux_sel

Mask-0				
Offset = 0x05				
Bit	R/W	Name	Reset Value	Description
7	R/W	Reserved	X	
6	R/W	BMC_to_HOST_INT_Mask	1	Mask to disable BMC-to-Host Interrupt.
5:1		Reserved	X	
0	R/W	TH_RESET_MASK	1	Mask to disable cpld_pcie_reset_n going to motherboard.

SKU ID				
Offset = 0x06				
Bit	R/W	Name	Reset Value	Description
7	RO	SKU_ID3	0	SKU ID[3:0] = 0000 0000 : Apache BW-DE CPU board 0001 : Reserved 0010 : Reserved : 1111 : Reserved
6	RO	SKU_ID2	0	
5	RO	SKU_ID1	0	
4	RO	SKU_ID0	0	
3	RO	HW_REV_ID1	1	Hardware Revision [1:0]= 10 00: Proto 01: Alpha 10: Beta 11: PVT
2	RO	HW_REV_ID0	1	
1	RO	BUILD_ID1	0	Build ID [1:0] = 00 00 : 1 01 : 2 10 : 3 11 : 4
0	RO	BUILD_ID0	0	

4.2 Main board CPLD Register Mapping and Description

CPLD1

Group	Offset	Register Name
Board information	0x00	Board Type and Revision
	0x01	Extend Board Type
	0x02	CPLD Revision Register
	0x03	CPLD ID Register
Port status	0x20-> NIF_QSFPDD P1 0x21-> NIF_QSFPDD P2 0x22-> NIF_QSFPDD P3 0x23-> NIF_QSFPDD P4 0x24-> NIF_QSFPDD P5 0x25-> NIF_QSFPDD P6 0x26-> NIF_QSFPDD P7 0x27-> NIF_QSFPDD P8 0x28-> NIF_QSFPDD P9 0x29-> NIF_QSFPDD P10 0x2A-> NIF_QSFPDD P11 0x2B-> NIF_QSFPDD P12	NIF_QSFPDD Port Status Register (Address 0x20~2B)
	0x2F	SFP+ Port0/1 Status Register
Port config	0x30-> NIF_QSFPDD P1 0x31-> NIF_QSFPDD P2 0x32-> NIF_QSFPDD P3 0x33-> NIF_QSFPDD P4 0x34-> NIF_QSFPDD P5 0x35-> NIF_QSFPDD P6 0x36-> NIF_QSFPDD P7 0x37-> NIF_QSFPDD P8 0x38-> NIF_QSFPDD P9 0x39-> NIF_QSFPDD P10 0x3A-> NIF_QSFPDD P11 0x3B-> NIF_QSFPDD P12	NIF_QSFPDD Port Model Select Register (Address 0x30~3B)
	0x3F	SFP+ Port0/1 Configuration Register
	0x40	Interrupt
	0x42	BMC Status
	0x43	BMC Watch Dog
	0x44	USB / PSU Status
	0x45	MUX control
	0x46 -> PUC[7:0] 0x47 -> PUC[15:8] 0x48 -> PUC[23:16] 0x49 -> PUC[29:24] 0x49 bit 7:6	BCM88690 PUC CPU/BMC Mux circuit setting

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Group	Offset	Register Name
	0x4A	Reset Control
	0x4B	33814/853S012 control
	0x4D / 0x4E	Reset Control with pulse output
	0x50	System LEDs Control Register 1
	0x51	System LEDs Control Register 2
	0x60 ~ 0x65	Thermal shutdown Status Register
	0x67	Thermal shutdown Register 1
	0x68	Thermal shutdown Register 2
	0x6F	Thermal shutdown Register 3

Board Type and Revision				
Offset	Bit Fields	Default	R/W	Description
0x00	D[1:0]	00	RO	Build REV [1:0] 00: P1, A1, B1, etc. 01: P2, A2, B2, etc. 10: P3, A3, B3, etc. 11: P4, A4, B4, etc.
	D[3:2]	00	RO	HW REV[1:0] Hardware Revision, defined by external resistors 00: Proto 01: Alpha 10: Beta 11: PVT
	D[7:4]	0000	RO	Model ID [3:0] 0100: S9700-23D others: Reserved

Extended Board Type				
Offset	Bit Fields	Default	R/W	Description
0x01	D[3:0]	0011	RO	Board ID [3:0] 0000~1111: Reserved for extended Board ID
	D[7:4]	0000	RO	Reserved

CPLD Revision Register				
Offset	Bit Fields	Default	R/W	Description
0x02	D[5:0]	000000	RO	CPLD code Revision Bit[5:0]: 000000: CPLD Code Revision is X.00 000001: CPLD Code Revision is X.01 000010: CPLD Code Revision is X.02 000011: CPLD Code Revision is X.03 ... 111111: CPLD Code Revision is X.63
	D[6]	0	RO	Release Bit: 0: CPLD Code is RD Revision 1: CPLD Code is Release Revision
	D[7]	0	RO	Reserved

CPLD ID Register				
Offset	Bit Fields	Default	R/W	Description
0x02	D[2:0]	000	RO	CPLD ID 000: CPLD 1 001: CPLD 2 010: CPLD 3 011: CPLD 4 100: CPLD 5
	D[7:3]	00000	RO	Reserved

NIF_QSFPDD Port Status Register (Address 0x20~2B)				
Offset	Bit Fields	Default	R/W	Description
Address mapping : 0x20-> P1 0x21-> P2 0x22-> P3 0x23-> P4 0x24-> P5 0x25-> P6 0x26-> P7 0x27-> P8 0x28-> P9 0x29-> P10 0x2A-> P11 0x2B-> P12	D[0]	1	RO	port A NIF_QSFPDD status (zQSFPD_INT#) 1= Port interrupt not exist 0= Port interrupt exist
	D[1]	1	RO	Port A NIF_QSFPDD Present (zQSFPD_ABS#) 1=Absent 0=Present
	D[2]	1	ROC	Port A QSFPDD Plug event 1=I/O without plugging 0=I/O with plugging
	D[7:3]	11111	RO	Reserved

SFP+ Port0/1 Status Register

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Offset	Bit Fields	Default	R/W	Description
0x2f	D[0]	1	RO	SFP+0 Present status 1=Absent 0=Present
	D[1]	1	RO	SFP+0 TX_Fault status 0=Normal 1=Tx fault
	D[2]	1	RO	SFP+ 0 RX_LOS status 1= Transceiver's optical side link down 0= Transceiver's optical side link up
	D[3]	1	RO	Reserved
	D[4]	1	RO	SFP+0 Present status 1=Absent 0=Present
	D[5]	1	RO	SFP+0 TX_Fault status 0=Normal 1=Tx fault
	D[6]	1	RO	SFP+ 0 RX_LOS status 1= Transceiver's optical side link down 0= Transceiver's optical side link up
	D[7]	1	RO	Reserved

NIF_QSFPDD Port Model Select Register (Address 0x30~3B)

Offset	Bit Fields	Default	R/W	Description
0x30-> P1 0x31-> P2 0x32-> P3 0x33-> P4 0x34-> P5 0x35-> P6 0x36-> P7 0x37-> P8 0x38-> P9 0x39-> P10 0x3A-> P11 0x3B-> P12	D[0]	1	RW	Port A NIF_QSFPDD RST# status (zQSFPx_RST#) 0: reset QSFP+ module 1: reset negated
	D[1]	1	RW	Reserved
	D[2]	0	RW	Port A NIF_QSFPDD LPMODE status (zQSFPx_LPMODE) 1= Low Power mode 0= High Power mode
	D[7:3]	11111	RW	Reserved

SFP+ Port0 Configuration Register

Offset	Bit Fields	Default	R/W	Description
0x3f	D[0]	0	RW	SFP+0 TXDIS status 0=Operating normally 1=Turned off
	D[1]	1	RW	controls the receive path signal rate capability

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SFP+ Port0 Configuration Register				
Offset	Bit Fields	Default	R/W	Description
				0: RX signal rate less than or equal to 4.25 GBd 1: RX signal rate greater than 4.25 GBd
	D[2]	1	RW	controls the transmit path signal rate capability 0: TX signal rate less than or equal to 4.25 GBd 1: TX signal rate greater than 4.25 GBd
	D[3]	1	RW	Reserve
	D[4]	0	RW	SFP+0 TXDIS status 0=Operating normally 1=Turned off
	D[5]	1	RW	controls the receive path signal rate capability 0: RX signal rate less than or equal to 4.25 GBd 1: RX signal rate greater than 4.25 GBd
	D[6]	1	RW	controls the transmit path signal rate capability 0: TX signal rate less than or equal to 4.25 GBd 1: TX signal rate greater than 4.25 GBd
	D[7]	1	RW	Reserved

Interrupt Register				
Offset	Bit Fields	Default	R/W	Description
0x40	D[0]	1	ROC	Port Interrupt (zQSFPx_INT#) 0=Port interrupt exist 1= Port interrupt not exist
	D[1]	1	RO	Reserved
	D[2]	0	RO	USB Over Current Protect(USB_OCP) 0 : USB is Over current 1 : USB is no over current
	D[3]	1	ROC	Port Present (zQSFPx_ABS#) 0= Port model insertion 1= Port model Not insertion
	D[4]	1	RO	PSU0 Interrupt (PSU0_INT_L) 0= Interrupt exist 1= Interrupt not exist
	D[5]	1	RO	PSU Interrupt (PSU1_INT_L) 0= Interrupt exist 1= Interrupt not exist
	D[6]	1	RO	PEX8724 Interrupt (PEX8724_INT_N) 0= Interrupt exist 1= Interrupt not exist
	D[7]	1	RO	CS4227 Interrupt (CS4227_INT_L) 0= Interrupt exist

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Interrupt Register				
Offset	Bit Fields	Default	R/W	Description
				1= Interrupt not exist

BMC Status Register				
Offset	Bit Fields	Default	R/W	Description
0x42	D[0]	0	RO	BMC present 0= BMC present 1= BMC absent
	D[6:1]	000000	RO	Reserved
	D[7]	1	RO	Thermal Status 0= Status output/Interrupt happen 1= Normal PS: depend on Thermal IC(U22/U31) setting..

Power Status Register				
Offset	Bit Fields	Default	R/W	Description
0x44	D[0]	0	RO	USB present 0= USB present 1= USB absent
	D[3:1]	000	RO	J2 ROV status
	D[4]	0	RO	PSU0 POWER OK 0= PSU0 power fail 1= PSU0 power ok
	D[5]	0	RO	PSU1 POWER OK 0= PSU1 power fail 1= PSU1 power ok
	D[6]	1	RO	PSU0 present 0= PSU0 present 1= PSU0 absent
	D[7]	1	RO	PSU1 present 0= PSU0 present 1= PSU0 absent

Mux Control Register				
Offset	Bit Fields	Default	R/W	Description
0x45	D[0]	0	RW	SFP0 I2C Mux 0= Disable 1= Enable
	D[1]	0	RW	SFP1 I2C Mux

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Mux Control Register				
Offset	Bit Fields	Default	R/W	Description
				0= Disable 1= Enable
	D[2]	0	RW	CPU read BMC id path 1 0= Disable 1= Enable
	D[3]	0	RW	CPU read BMC id path 2 0= Disable 1= Enable
	D[5:4]	00	RW	Reserved
	D[6]	0	RW	BMC_MUX_SEL 0: I2C_BMC bus from I2C2_BMC 1: I2C_BMC bus from HOST_I2C0
	D[7]	1	RW	CPU_MUX_SEL 0: I2C_CPU bus from I2C1_BMC 1: I2C_CPU bus from HOST_I2C0

Reset Control Register				
Offset	Bit Fields	Default	R/W	Description
0x4A	D[0]	1	RW	Software Reset 0= Reset system 1= Normal
	D[1]	0	RW	CP2104 Reset 0= Normal 1= Reset CP2104
	D[2]	1	RW	Reserved
	D[3]	1	RW	BMC Reset 0= Reset BMC 1= Normal
	D[4]	1	RW	BMC LPC Reset 0= Reset LPC of BMC 1= Normal
	D[5]	1	RW	I210 Reset 0= Reset I210 1= Normal
	D[7:6]	11	RW	Reserved

Reset Control Register 2				
Offset	Bit Fields	Default	R/W	Description
0x4D	D[0]	1	RW	OP2 CRST_L Reset 0= Reset OP2 CRST_L 10mS

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Reset Control Register 2				
Offset	Bit Fields	Default	R/W	Description
				1= Normal
	D[1]	1	RW	OP2 PERST Reset 0= Reset OP2 PERST_L 110mS 1= Normal
	D[2]	1	RW	OP2 SRST_L Reset 0= Reset OP2 SRST_L 10mS 1= Normal
	D[3]	0	RW	82P33814 Reset 0= Reset 82P33814 80mS 1= Normal Reference: CPLD_RESET_N
	D[4]	0	RW	CS4227 Reset 0= Reset CS4227 2mS 1= Normal
	D[5]	1	RW	Reserved
	D[6]	1	RW	Reserved
	D[7]	0	RW	PEX8724 Reset 0= Reset PEX8724 10mS 1= Normal Reference: RST_PCIE_CPU_TO_MB_N

CPLD2/3

Group	Offset	Register Name
Board information	0x02	CPLD Revision Register
	0x03	CPLD ID Register
Port status	CPLD2: 0x2A-> FAB_QSFPDD P1 0x2B-> FAB_QSFPDD P2 0x2C-> FAB_QSFPDD P3 CPLD3: 0x20-> FAB_QSFPDD P4 0x21-> FAB_QSFPDD P5 0x22-> FAB_QSFPDD P6 0x23-> FAB_QSFPDD P7 0x24-> FAB_QSFPDD P8 0x25-> FAB_QSFPDD P9 0x26-> FAB_QSFPDD P10	FAB_QSFPDD Port Status Register (Address 0x20~2C)

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Group	Offset	Register Name
	0x27-> FAB_QSFPDD P11 0x28-> FAB_QSFPDD P12 0x29-> FAB_QSFPDD P13 0x2A-> FAB_QSFPDD P14	
Port configuration	CPLD2: 0x3A-> FAB_QSFPDD P1 0x3B-> FAB_QSFPDD P2 0x3C-> FAB_QSFPDD P3 CPLD3: 0x30-> FAB_QSFPDD P4 0x31-> FAB_QSFPDD P5 0x32-> FAB_QSFPDD P6 0x33-> FAB_QSFPDD P7 0x34-> FAB_QSFPDD P8 0x35-> FAB_QSFPDD P9 0x36-> FAB_QSFPDD P10 0x37-> FAB_QSFPDD P11 0x38-> FAB_QSFPDD P12 0x39-> FAB_QSFPDD P13 0x3A-> FAB_QSFPDD P14	FAB_QSFPDD Port Model Select Register (Address 0x30~3C)
	0x40	Port Interrupt
FAB_400G LED Control	0x80-> FAB_QSFPDD LED 1 、 2 0x81-> FAB_QSFPDD LED 3 、 4 0x82-> FAB_QSFPDD LED 5 、 6 0x83-> FAB_QSFPDD LED 7 、 8 0x84-> FAB_QSFPDD LED 9 、 10 0x85-> FAB_QSFPDD LED 11 、 12 0x86-> FAB_QSFPDD LED 13 、 14	QSFPDD LED control Register (Address 0x80~86) Only for CPLD3

CPLD Revision Register				
Offset	Bit Fields	Default	R/W	Description

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CPLD Revision Register				
Offset	Bit Fields	Default	R/W	Description
0x02	D[5:0]	000000	RO	CPLD code Revision Bit[5:0]: 000000: CPLD Code Revision is X.00 000001: CPLD Code Revision is X.01 000010: CPLD Code Revision is X.02 000011: CPLD Code Revision is X.03 ... 111111: CPLD Code Revision is X.63
	D[6]	0	RO	Release Bit: 0: CPLD Code is RD Revision 1: CPLD Code is Release Revision
	D[7]	0	RO	Reserved

CPLD ID Register				
Offset	Bit Fields	Default	R/W	Description
0x03	D[2:0]	001	RO	CPLD ID 000: CPLD 1 001: CPLD 2 010: CPLD 3 011: CPLD 4 100: CPLD 5
	D[7:3]	00000	RO	Reserved

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FAB_QSFPDD Port Status Register (Address 0x2A~2C) for CPLD2				
Offset	Bit Fields	Default	R/W	Description
0x2A-> FAB_QSFPDD P1 0x2B-> FAB_QSFPDD P2 0x2C-> FAB_QSFPDD P3	D[0]	1	RO	Port x FAB_QSFPDD status (zQSFPx_INT#) 1= Transceiver's optical side link down 0= Transceiver's optical side link up
	D[1]	1	RO	Port x FAB_QSFPDD Present status (zQSFPx_ABS#) 1=Absent 0=Present
	D[2]	1	ROC	Port A QSFPDD Plug event 1=I/O without plugging 0=I/O with plugging
	D[3]	1	RO	Reserved
	D[4]	1	RO	Reserved
	D[5]	1	RO	Reserved
	D[6]	1	RO	Reserved
	D[7]	1	RO	Reserved

FAB_QSFPDD Port Status Register (Address 0x20~2A) for CPLD3				
Offset	Bit Fields	Default	R/W	Description
0x20-> FAB_QSFPDD P4 0x21-> FAB_QSFPDD P5 0x22-> FAB_QSFPDD P6 0x23-> FAB_QSFPDD P7 0x24-> FAB_QSFPDD P8 0x25-> FAB_QSFPDD P9 0x26-> FAB_QSFPDD P10 0x27-> FAB_QSFPDD P11 0x28-> FAB_QSFPDD P12 0x29-> FAB_QSFPDD P13 0x2A-> > FAB_QSFPDD P14	D[0]	1	RO	Port x QSFP28/QSFPDD status (zQSFPx_INT#) 1= Transceiver's optical side link down 0= Transceiver's optical side link up
	D[1]	1	RO	Port x QSFP28/QSFPDD Present status (zQSFPx_ABS#) 1=Absent 0=Present
	D[2]	1	ROC	Port A QSFPDD Plug event 1=I/O without plugging 0=I/O with plugging
	D[3]	1	RO	Reserved
	D[4]	1	RO	Reserved
	D[5]	1	RO	Reserved
	D[6]	1	RO	Reserved
	D[7]	1	RO	Reserved

FAB_QSFPDD Port Model Select Register (Address 0x3A~3C) for CPLD2				
Offset	Bit Fields	Default	R/W	Description

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FAB_QSFPDD Port Model Select Register (Address 0x3A~3C) for CPLD2				
Offset	Bit Fields	Default	R/W	Description
0x3A-> FAB_QSFPDD P1 0x3B-> FAB_QSFPDD P2 0x3C-> FAB_QSFPDD P3	D[0]	1	RW	Port x FAB_QSFPDD RST# status (zQSFPx_RST#) 0: reset QSFP+ module 1: reset negated
	D[1]	1	RW	Reserved
	D[2]	0	RW	Port x FAB_QSFPDD LPMODE status (zQSFPx_LPMODE) 1= Low Power mode 0= High Power mode
	D[3]	1	RW	Reserved
	D[4]	1	RW	Reserved
	D[5]	1	RW	Reserved
	D[6]	1	RW	Reserved
	D[7]	1	RW	Reserved

FAB_QSFPDD Port Model Select Register (Address 0x3A~3C) for CPLD2				
Offset	Bit Fields	Default	R/W	Description
0x3A-> FAB_QSFPDD P1 0x3B-> FAB_QSFPDD P2 0x3C-> FAB_QSFPDD P3	D[0]	1	RW	Port x FAB_QSFPDD RST# status (zQSFPx_RST#) 0: reset QSFP+ module 1: reset negated
	D[1]	1	RW	Reserved
	D[2]	0	RW	Port x FAB_QSFPDD LPMODE status (zQSFPx_LPMODE) 1= Low Power mode 0= High Power mode
	D[3]	1	RW	Reserved
	D[4]	1	RW	Reserved
	D[5]	1	RW	Reserved
	D[6]	1	RW	Reserved
	D[7]	1	RW	Reserved

FAB_QSFPDD Port Model Select Register (Address 0x30~3A) for CPLD3				
Offset	Bit Fields	Default	R/W	Description
0x30-> FAB_QSFPDD P4 0x31-> FAB_QSFPDD P5 0x32-> FAB_QSFPDD P6 0x33-> FAB_QSFPDD P7 0x34-> FAB_QSFPDD P8 0x35-> FAB_QSFPDD P9 0x36-> FAB_QSFPDD P10	D[0]	1	RW	Port x FAB_QSFPDD RST# status (zQSFPx_RST#) 0: reset QSFP+ module 1: reset negated
	D[1]	1	RW	Reserved
	D[2]	0	RW	Port x FAB_QSFPDD LPMODE status (zQSFPx_LPMODE)

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FAB_QSFPDD Port Model Select Register (Address 0x30~3A) for CPLD3				
Offset	Bit Fields	Default	R/W	Description
0x37-> FAB_QSFPDD P11				1= Low Power mode
0x38-> FAB_QSFPDD P12				0= High Power mode
0x39-> FAB_QSFPDD P13	D[3]	1	RW	Reserved
0x3A-> FAB_QSFPDD P14	D[4]	1	RW	Reserved
	D[5]	1	RW	Reserved
	D[6]	1	RW	Reserved
	D[7]	1	RW	Reserved

Port Interrupt Register				
Offset	Bit Fields	Default	R/W	Description
0x40	D[0]	1	RW	Port Interrupt 0=Port interrupt exist 1= Port interrupt not exist
	D[1]	1	RW	Reserved
	D[2]	1	RW	Reserved
	D[3]	1	RW	Reserved
	D[4]	1	RW	Reserved
	D[5]	1	RW	Reserved
	D[6]	1	RW	Reserved
	D[7]	1	RW	Reserved

Port QSFPDD LED0~LED13 Status				
Offset	Bit Fields	Default	R/W	Description
0x80: Port 0~1 0x81: port 2~3 0x82: Port 4~5 0x83: port 6~7 0x84: Port 8~9 0x85: port 10~11 0x86: Port 12~13	D[0]	0	RW	Port x LED Status 1: Yellow On 0: Yellow Off
	D[1]	0	RW	Port x LED Status 1: Green On 0: Green Off
	D[2]	0	RW	Port x LED Status 1: Blue On 0: Blue Off
	D[3]	0	RW	Port x LED Blinking 1: Blinking 0: keep the Status
	D[4]	0	RW	Port (x+1) LED Status 1: Yellow On 0: Yellow Off
	D[5]	0	RW	Port (x+1) LED Status 1: Green On 0: Green Off
	D[6]	0	RW	Port (x+1) LED Status

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Port QSPDD LED0~LED13 Status				
Offset	Bit Fields	Default	R/W	Description
				1: Blue On 0: Blue Off
	D[7]	0	RW	Port (x+1) LED Blinking 1: Blinking 0: keep the Status